

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

IN RE APPLICATION OF: Akira UMEZAWA, et al.

SERIAL NO: NEW APPLICATION

GAU:

FILED: HEREWITH

EXAMINER:

FOR: SEMICONDUCTOR MEMORY DEVICE INCLUDING MOS TRANSISTORS EACH HAVING A FLOATING GATE AND A CONTROL GATE

**INFORMATION DISCLOSURE STATEMENT UNDER 37 CFR 1.97**

COMMISSIONER FOR PATENTS  
ALEXANDRIA, VIRGINIA 22313

SIR:

Applicant(s) wish to disclose the following information.

**REFERENCES**

- ☒ The applicant(s) wish to make of record the references listed on the attached form PTO-1449. Copies of the listed references are attached, where required, as are either statements of relevancy or any readily available English translations of pertinent portions of any non-English language references.
- ☐ A check or credit card payment form is attached in the amount required under 37 CFR §1.17(p).

**RELATED CASES**

- ☐ Attached is a list of applicant's pending application(s) or issued patent(s) which may be related to the present application. A copy of the patent(s), together with a copy of the claims and drawings of the pending application(s) is attached along with PTO 1449.
- ☐ A check or credit card payment form is attached in the amount required under 37 CFR §1.17(p).

**CERTIFICATION**

- ☐ Each item of information contained in this information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of this statement.
- ☐ No item of information contained in this information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application or, to the knowledge of the undersigned, having made reasonable inquiry, was known to any individual designated in 37 CFR §1.56(c) more than three months prior to the filing of this statement.

**DEPOSIT ACCOUNT**

- ☒ Please charge any additional fees for the papers being filed herewith and for which no check or credit card payment is enclosed herewith, or credit any overpayment to deposit account number 15-0030. A duplicate copy of this sheet is enclosed.

Respectfully submitted,

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**STATEMENT OF RELEVANCY**

**Reference AA (U.S. 6,256,227 B1) on Form PTO-1449:**

A NOR flash memory design is described with hierarchical bit line decoding architecture. This core architecture is preferable to embedded flash required to head fast at random. The objective is to reduce parasitic capacitance of read path so that high speed access is achieved.

**Reference AB (U.S. 6,222,774 B1) on Form PTO-1449:**

FN-Erase operation with negative voltage is claimed. To conquer the problem of excess voltage stress over decoders and PN forward bias causing latch-up, when erase operation finishes, terminals of work lines and substrates are electrically shorted after the terminals are set to floating bias condition.

Form PTO 1449  
(Modified)U.S. DEPARTMENT OF COMMERCE  
PATENT AND TRADEMARK OFFICEATTY DOCKET NO.  
247512US2SSERIAL NO.  
NEW APPLICATIONS

## LIST OF REFERENCES CITED BY APPLICANT

APPLICANT  
Akira UMEZAWA, et al.FILING DATE  
HEREWITH

GROUP

## U.S. PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS	FILING DATE IF APPROPRIATE
	AA	6,256,227 B1	07/03/01	Shigeru ATSUMI, et al.			
	AB	6,222,774 B1	04/24/01	Toru TANZAWA, et al.			
	AC						
	AD						
	AE						
	AF						
	AG						
	AH						
	AI						
	AJ						
	AK						
	AL						
	AM						
	AN						

## FOREIGN PATENT DOCUMENTS

		DOCUMENT NUMBER	DATE	COUNTRY	TRANSLATION	
					YES	NO
	AO					
	AP					
	AQ					
	AR					
	AS					
	AT					
	AU					
	AV					

## OTHER REFERENCES (Including Author, Title, Date, Pertinent Pages, etc.)

	AW	
	AX	
	AY	
	AZ	

☐ Additional References sheet(s) attached

Examiner

Date Considered

\*Examiner: Initial if reference is considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.